CLAIMS

1. A content addressable arrayed control system, comprising a plurality of control cells each comprising a plurality of memory cells, each memory cell receiving a respective one of a plurality of data lines distributed to all of said control cells and a respective one of a plurality of timing lines distributed to all of said control cells, and a load line distributed only to one of the control cells of said plurality of control cells, each memory cell comprising:

a 1-bit latch triggered by said load line to latch a signal on said respective data line; and

a 1-bit comparator comparing an output of said latching circuit with a signal on said respective timing line and outputting a valid bit compare signal on an output line commonly connected to the comparators of all memory cell of said control cell, an address compare signal on said output line being valid only when all of said comparators of said control cell output valid bit compare signals.

2. The system of Claim 1, wherein each control cell further includes an output latch latching in response to said output signal a state signal on a state line distributed to all output latches of said said plurality of control cells.

3. The system of Claim 2, further comprising a counter driven by a clock signal having a high-order bit driving said state line and lower-order bits driving respective ones of said timing lines.

4. The system of Claim 3, further comprising an address decoder receiving a multi-bit address signal and enabling in response thereto only one of said load lines.

5. The system of Claim 3, wherein count intervals of said counter are non-uniform in duration.

6. A content addressable control section for controlling N time delays supplied to a plurality N of drive sections, comprising:

a multi-bit data bus;

N registers seletively connected in parallel to said data bus;

at least one control line connected to said N registers to reset said registers according to data on said data bus; and

a single clocked counter connected to respective ones of said registers and providing an output in comparision to said connected registers.

7. The control section of Claim 6, wherein said trigger signal is synchronous with a clock signal.

8. The control section of Claim 6, wherein said trigger signal is aperiodic.

9. The control section of Claim 6, wherein said registers and counters are arranged in rows and columns and wherein seach of registers is controlled by a row enable signal, a column enable signal, and a load signal.